Foundation IP for IoT and Mobile Applications on TSMC 40ULP

Synopsys

TSMC 2016
Open Innovation Platform®
Ecosystem Forum

ABSTRACT

With TSMC close to qualifying eFlash at 40nm, the 40nm node will soon become the preferred node for SoCs targeting Internet of Things (IoT) applications.

TSMC's 40ULP process technology provides the lowest dynamic and standby power needed for IoT and mobile applications when combined with a Foundation IP portfolio of logic libraries and memory compilers, as well as non-volatile memory (NVM), that can take advantage of these unique process features. The process provides a new eHVT device for >70% leakage reduction, 0.9V operation for >30% less active power consumption, new ULL SRAM bitcells and compatibility with existing 1.1V 40LP IP.

This presentation will provide details on how designers of IoT applications can combine the benefits of the TSMC 40ULP process with Synopsys' portfolio of logic libraries, embedded memories with test and repair, and Multi Time Programmable (MTP) NVM to achieve their power, performance and area targets.

It will describe:

- Why the 40nm process is gaining traction in IoT applications
- How memory compliers can support the lowest operating voltages by leveraging assist circuitry
- How the memories' power management capabilities can be used to reduce IoT SoC power consumption
- How logic libraries can use low-power circuits, such as multi-bit flip flops, to achieve the lowest active power and how the circuits can be extended for near threshold operation
- How ultra-low leakage libraries can be used to build always-on logic blocks, reducing leakage by up to 100X
- How always-on logic blocks can connect directly to a wide variety of energy sources with and without voltage regulators
- A brief overview of Synopsys' additional IP solutions for the TSMC 40ULP process, including interface IP, NVM, and memory and system hierarchical test solutions

SYNOPSYS® Silicon to Software™

Foundation IP for IoT and Mobile Applications on TSMC 40ULP

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Agenda

Growth of IoT Edge Device Applications

Energy Efficiency

Foundation IP for IoT

- Low Power Logic
- Low Power Memories

Summary

From the Edge to the Cloud

IoT Edge Devices
(Smart Devices)

"Things" with sensors & actuators that monitor and control

Aggregation Layers
(Hubs/Gateways)

Connectivity & Interfaces to aggregate the edge data to send to the cloud

Remote Processing
(Cloud Based)

Applications to analyze the data and offer cloud services

IoT Edge Device Market

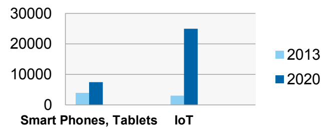
Internet of Things and its Attractive Growth…

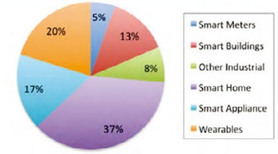
- 5B people connected by 2020[1]
- 33B objects connected by 2020, IoT will include 25B[2] (~2Bu/yr)
- 11.5% CAGR through 2022 for IoT Chip Market (from $4.6 to $10.8B)[3]
- 50%+ volume driven by Smart Home and Wearables[5]
- 55% global IoT security market growth through 2019[4]
- $7.4B and over 887 deals to IoT startups since 2010[6]

Fragmented Market….. So key applications drive innovation

- Mobile handsets drive interoperability (WiFi, Cellular, Bluetooth)
- Regulations & Standards drive security (PCI, NIST, FIPS, Common Criteria, WiFi, etc)
- Wearables & Drones drive energy efficiency

Billions of "Things" in use*





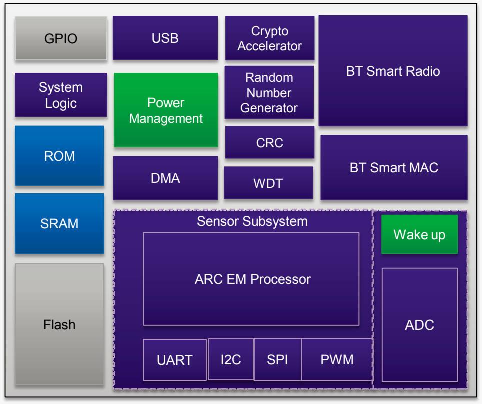
2021: 2.2 billion units

Figure 4-1. IoT unit share by market segment, 2021. We project the consumer-driven smart home and wearables segments to be the largest contributors. (Source: The Linley Group)

Source[1]: World Economic Forum
Source[2]: Gartner
Source[3]: Marketandmarkets
Source[4]: Marketresearchrports.biz
Source[5]: Linley 2016 IoT Report
Source[6]: CB Insights

Wearable Fitness & Health SoC

Example SOC Block Diagram



- Built with Logic Libraries/Analog
- Always On
- Memory
- Foundry IP

Energy Efficiency of Logic Libraries and Memories Affects IoT Blocks

Energy Efficiency

Energy Efficiency

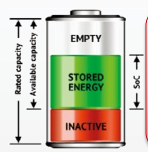
Energy Costs Require Innovation

- Gigantic batteries, getting bigger

- Space & cost constrained
- Increased capabilities
- Power is everything!

Increasing Battery Size can cost more than entire SOC

225 mAh CR2032	$1.33
1Ah CR2477	$4.76
1320mAh LiPo	$11.99
2100mAh LiPo	$18.97



Batteries age over 20-30 years

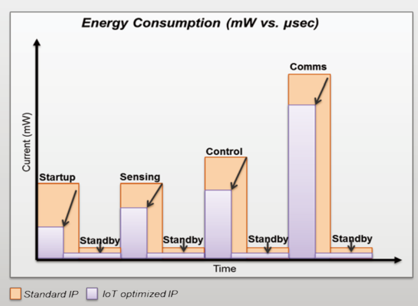
Device	Power	Battery	Duration
Google Glass	570mAh	Li Polymer	1 days
Huawei Watch	300mAh	Li-Ion	2 days
Garmin VivoSmart HR	205mAh	Li-Ion	5 days
Starkey Hearing Aid	91- 630mAh	Zinc Air	3-22 days

Off-the-shelf vs Custom ASIC: Other wearables can benefit from innovation found in hearing aids

Power Profile Reduction

Leveraging Yesterday's Foundation IP will not Compete

Example Case



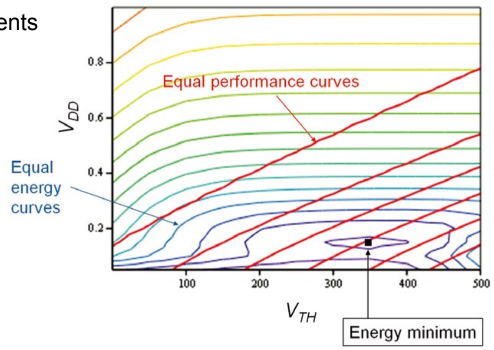
Improving Energy Efficiency

- Reduce Voltage
- Reduce Leakage
- Reduce Die Size
- Reduce Cycle Count
- Reduce Frequency

Challenges of Near Threshold Computing

Accurate Foundry Models are Critical for Low-Voltage Operation

- Achieving Device Specifications
  - Meet throughput requirements
  - Duty cycle optimization
- Energy Minimization
  - Finding the inflection point
  - Optimal energy tradeoffs
- Custom PVT Modeling
  - Slow waveforms
  - Managing transitions
  - Multiple voltage domains
- Modeling Issues
  - Clock trees
  - Increasing variability at low voltages



Source: Dr. Jan M. Rabaey, Low Power Essentials

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Foundation IP for IoT

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Synopsys Low Power IP Solutions for IoT

Memories & Libraries

- Ultra high-density, always-on logic libraries
- Low voltage support
- Embedded test & repair supporting Flash

Subsystem IP

- Integrated HW & SW subsystem
- Ultra low power sensor subsystem for sensor fusion

Processor Cores

- ARC HS for higher-end IoT
- ARC EM for low-power IoT
- ASIP – App. specific processors

NVM, Analog & Interface IP

- Bluetooth Smart IP
- Data Converters
- USB, DDR, MIPI
- Non-Volatile Memory

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Synopsys Logic Libraries for TSMC 40ULP

*Broad Selection for Optimal PPA & Process Tradeoffs – **Foundry Sponsored***

Performance	Power	Area
• 9 Track libraries built for GHz operation • Fast flip-flops with variable setup take advantage of useful skew • Clock drivers & clock gates minimize uncertainty	• 7 Track libraries with long channel variants in extreme high VT (eHVT) for lowest power • POK minimizes core leakage: power gates, level shifters, always-on, retention flops, isolation cells	• 7 Track library provides highest density and lowest power • Multi-bit flip flops, high density flops and combinational cells with high pin accessibility for densest block routes

- ~1,700 to 2,500 cells per architecture designed for highest routed density
- HPC Design Kit with special cells for performance, power and area of CPU/GPU/DSP
- Power Optimization Kits for block shut down, DVFS
- Characterized at multiple sets of PVTs in multiple VT/channel length combinations on multiple processes

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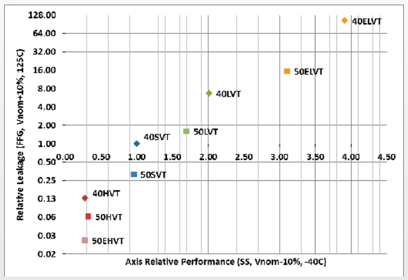
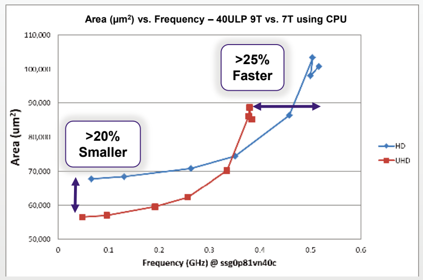
DesignWare Logic Libraries for TSMC 40ULP Deliver Best PPA

Broad Offering of Libraries & Views Provides Complete SoC Design Platform

Wide range of VTs, channel lengths and PVTs enable PPA tradeoffs for the entire SoC (40ULP 7 Track Library)



HPC Design Kit libraries for 7 and 9 track deliver significant performance boost and area savings



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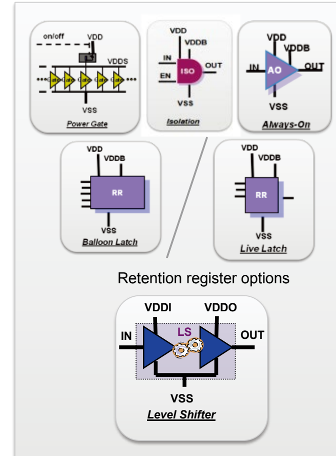
DesignWare Power Optimization Kit

Minimize Core Leakage

- Eliminate leakage in idle blocks
  - Shut down idle blocks (sleep mode)
  - Needs: Power gates, isolation cells
- Maximize idle block leakage reduction with quick "naps"
  - State retention in sleep mode enables fast shut-down and wake-up
  - Needs: Retention registers, always on cells, isolation cells
- Multiple Voltage Domains
  - DVS, DFS, DVFS
  - Needs: Level Shifters
- Lower leakage in active mode
  - Low leakage cells in non-critical paths
  - Needs: Multi-VT base cells



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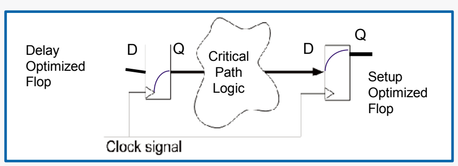
Specialty Flip-Flops Stretch Performance at Low Voltages & Minimize Power

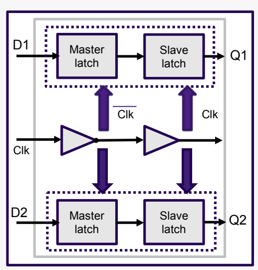
Multiple Flop Variants Enable Targeted Optimization

Performance



Delay optimized and setup optimized flops manage critical logic paths

Power



Multi-bit flops minimize clock loading, area and leakage

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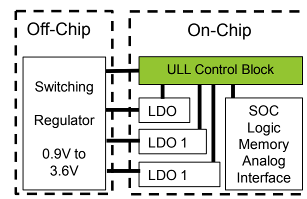
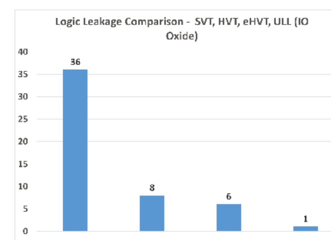
Ultra Low Leakage (Thick Oxide) Library

- Lowest leakage for always-on wakeup circuits
  - Up to 36X lower leakage of thin oxide cells
- Library contains >200 cells with >70 functions
  - 12 track architecture for large Lg devices
  - Combinational circuits for boolean functions
  - Sequential (flip-flops) with retention
  - Clock cells
  - Level shifters to core voltage PVTs
  - Isolation cells for managing power down
  - Routing kit - fillers, endcaps, DCAPs
- Supports operation from 0.9V to 3.6V
  - High voltage capability for use without regulators
  - Uses 2.5V (3.3VOD) IO Oxide





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EDA Track
IP Track
EDA / IP / Services Track
Print-Only Papers

PVTs To Manage Power Domains

#	Process	Voltage	Temp
1	TT	0.9	25
2	TT	0.9	85
3	TT	1.1	25
4	TT	1.1	85
5	FFG	0.99	85
6	FFG	0.99	125
7	FFG	0.99	-40
8	SSG	0.81	85
9	SSG	0.81	125
10	SSG	0.81	-40
11	FF	0.99	85
12	FF	0.99	125
13	FF	0.99	-40
14	SS	0.81	85
15	SS	0.81	125
16	SS	0.81	-40
17	FFG	1.21	85
18	FFG	1.21	125
19	FFG	1.21	-40
20	SSG	0.99	85
21	SSG	0.99	125
22	SSG	0.99	-40
23	FF	1.21	85
24	FF	1.21	125
25	FF	1.21	-40
26	SS	0.99	85
27	SS	0.99	125
28	SS	0.99	-40

9T and 7T

#	Process	Voltage	Temp
1	TT	1.0V	25C
2	TT	1.0V	85C
3	FFG	1.1V	85C
4	FFG	1.1V	125C
5	FFG	1.1V	-40C
6	SSG	0.9V	85C
7	SSG	0.9V	125C
8	SSG	0.9V	-40C
9	FF	1.1V	85C
10	FF	1.1V	125C
11	FF	1.1V	-40C
12	SS	0.9V	85C
13	SS	0.9V	125C
14	SS	0.9V	-40C

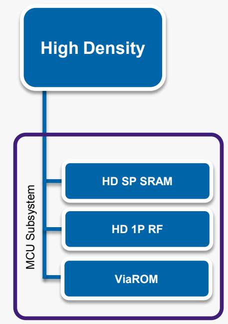
9T

Same PVTs for Logic Libraries and Memory Compilers

Active Power ~ CFV^2

*Custom PVTs available by request can be quoted

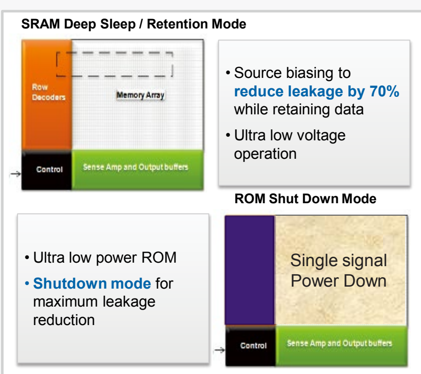
DesignWare Memory Compilers for IoT



- IoT needs high density, low leakage memory with power reduction modes
  - High Density Single Port SRAM
  - High Density Single Port Register File
  - Ultra Low Leakage ViaROM
- Bringing advanced power management to 40nm
  - Leakage savings w/ DeepSleep/retention mode with single pin control: 70% leakage reduction
  - Long channel devices to reduce active leakage
  - Ultra low voltage operation by using assist circuitry: 0.9V support at 40nm eFlash
  - Ultra low power zero-array viaROM reducing leakage more than 20%

Low Power DesignWare SRAMs and ROMs

Ideal for IoT Devices

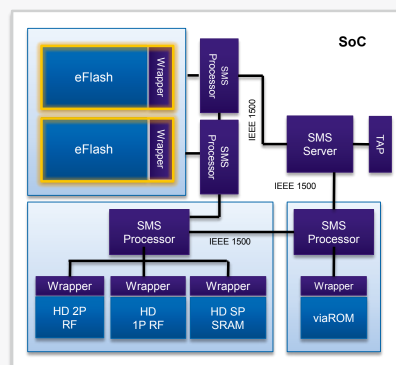


- Bringing advanced power management design techniques to mature nodes
  - Robust low voltage SRAM operation with assist circuitry (0.9V @ 40nm)
  - DeepSleep retention mode for 70% leakage reduction
  - Aggressive use of long channel devices
- Zero-array ROM for further power reduction; zero array leakage
- Shutdown mode with integrated power gates

Convenient to Have Power Modes Controlled by a Single Pin

DesignWare STAR Memory System

Embedded & External Memory Test, Repair and Diagnostics



- High quality test & repair for eFlash
  - Small footprint BIST with lower cost than external FPGA testing
  - Comprehensive BIST patterns based on technology specific failure pareto charts
  - On-chip repair across multiple corners
  - Supports multiple macros & shared wrappers
- Seamless integration with Yield Accelerator and Silicon Browser
- Award winning debug and diagnosis ecosystem

Supports TSMC 40nm eFlash

DesignWare Foundation IP for TSMC 40nm

Reducing Power Consumption & Leakage for IoT Applications

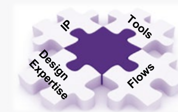
Logic Libraries	40LP	40ULP
High Density 9-Track	HVT, SVT, LVT	• >30% lower active power • >70% lower standby power • 250 additional cells for backward compatibility; multi-bit flip-flops and other low-power circuits • eHVT, HVT, SVT, LVT, eLVT available
Ultra High Density 7-Track	n/a	• >20% lower area and power than 9-track • Multi-bit flip-flops and other low-power circuits • eHVT, HVT, SVT, LVT, eLVT available
Ultra Low Leakage Thick Oxide	n/a	• Thick oxide cuts leakage by 95% compared to thin oxide; can withstand up to 3.6V for direct LiON battery connection

Embedded Memories	40LP	40ULP (1.1V)	40ULP (0.9V)
16K x 32 bits • HD SP SRAM • 1P Register Files • 1MB Via ROM	• SVT, LVT • Light sleep, deep sleep, shutdown	• 52% lower leakage • 50nm channel lengths • eHVT, SVT • Light sleep, deep sleep, shutdown	• 65% lower leakage • Read & write assist for low voltages • 50nm channel length • eHVT, SVT • Light sleep, deep sleep, shutdown

40LP eFlash & 40ULP eFlash Coming Soon

Summary

- 40nm is an attractive node for IoT devices now that low power Foundation IP and high density eFlash is available
- Required frequency, activity profile, available voltages and the right IP can minimize total power
- Logic power can be minimized by choices in:
  - Logic Design
  - Logic Library Design
  - EDA Tools and Flow



- Memory power can be minimized by choices in:
  - Memory Compilers
  - Instance Configurations
- In crowded IoT space, he or she who achieves the lowest power, wins

Q&A

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